**Design and implementation of half adder**

**Objective: A half adder is a type of adder to add the input signal and find the output for the ‘Sum’ and “Carry” value. It can be constructed for many number representations such as BCD(binary coded decimal), the most common adders operate on binary numbers.**

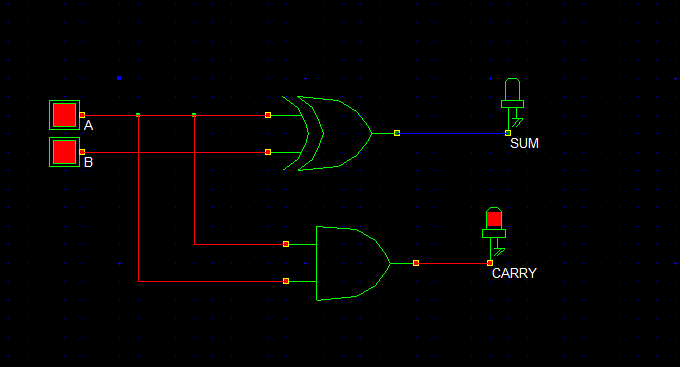
**Theory:**

A half adder add the 2 input and results into a two-digit output. Two output such as SUM(S) and CARRY(C). It may represented such as XOR logic gate and an AND logic gate. The Boolean logic for the sum will be *A′B* + *AB′* and carry(AB).

**Truth Table**

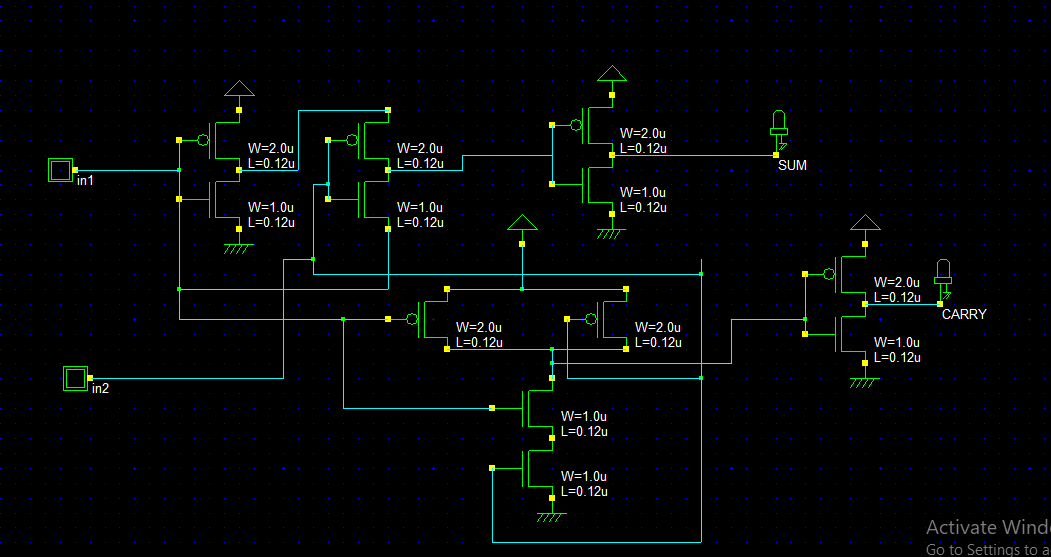
|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **SUM** | **CARRY** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |

**1)Using XOR gate and And gate circuit diagram**

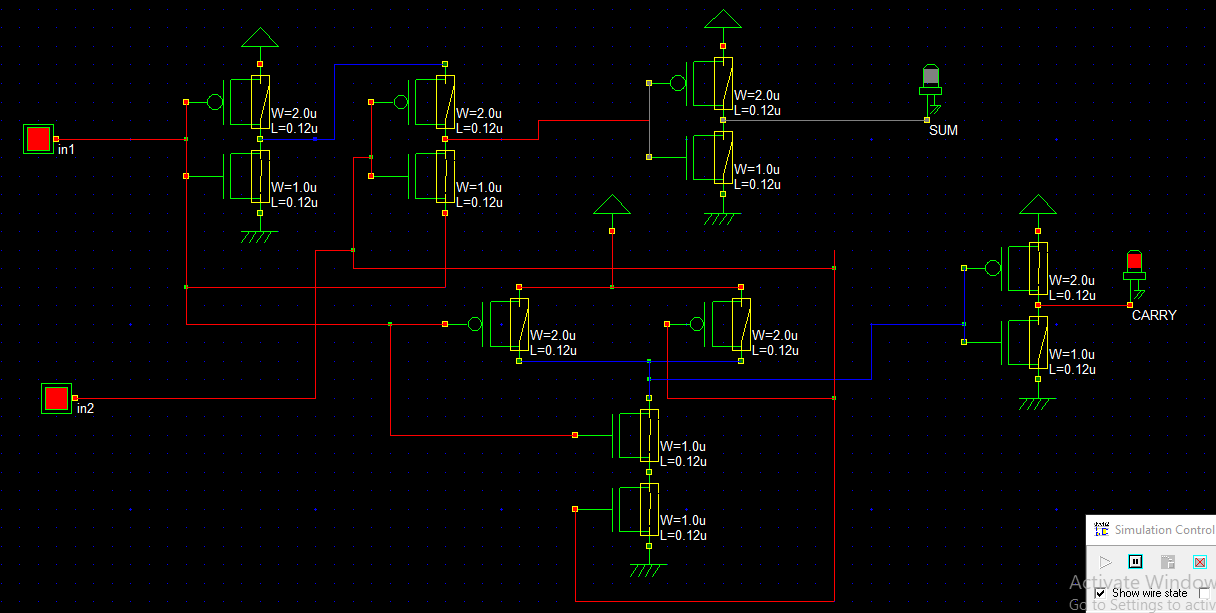
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**2)Circuit Diagram**

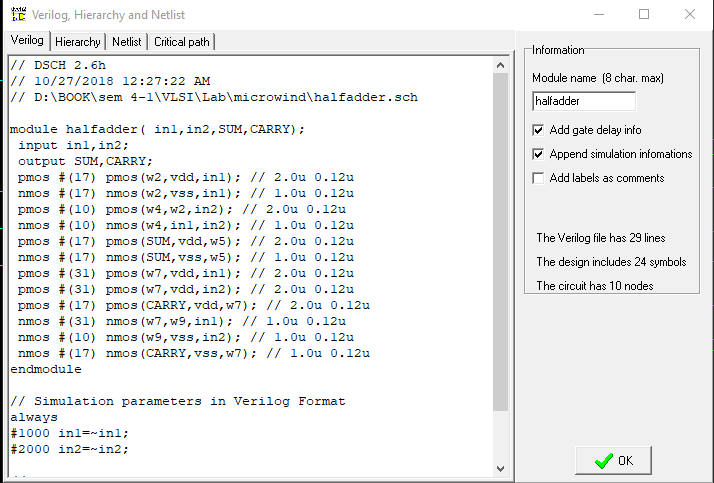
If in1 and in2 is 0 ,then the output will be

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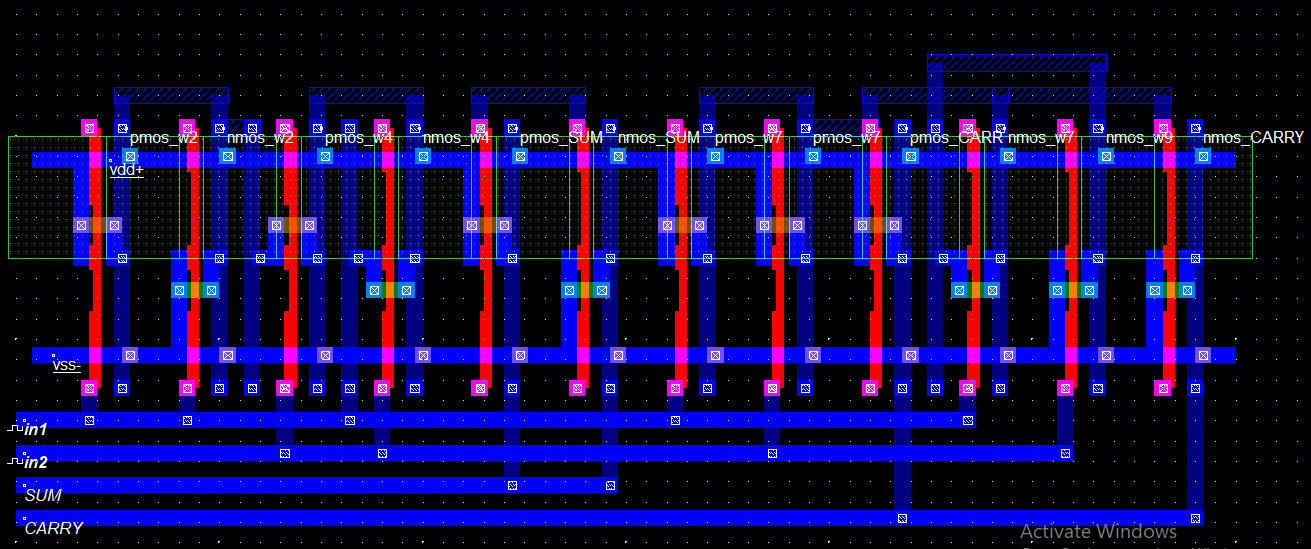
If in1 and in2 is 1,then

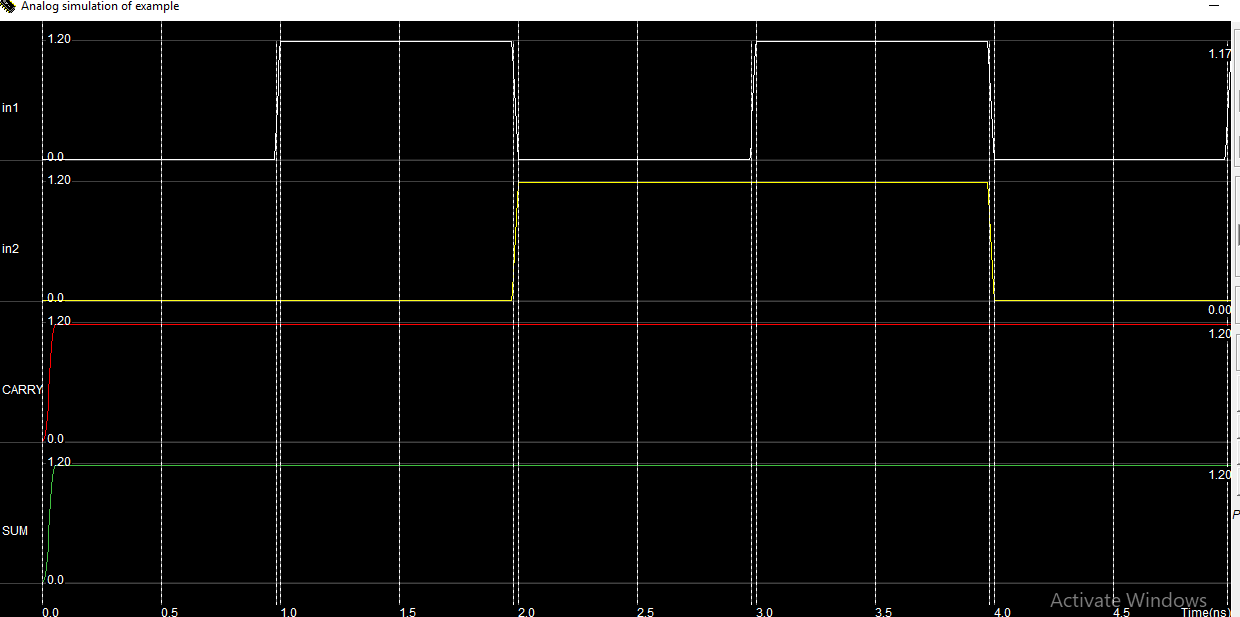


**Verilog File**

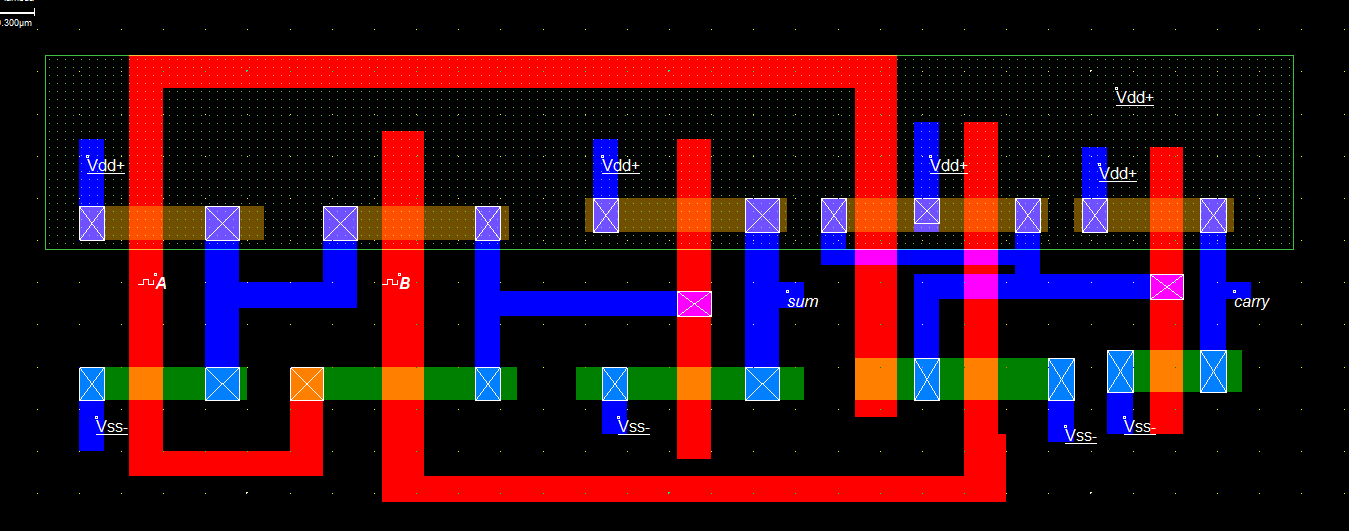
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**Layout**

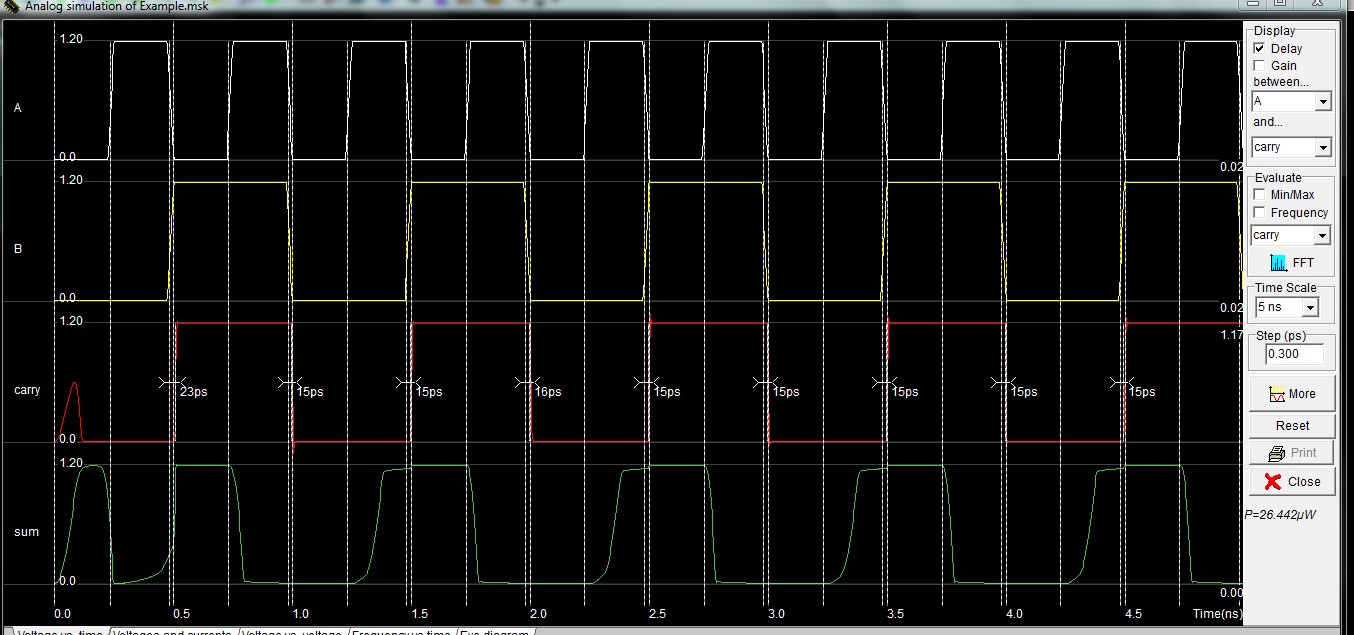
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**Layout Timing Diagram**

**Stick Diagram**



**Timing Diagram**



**Discussion:**

The ALU of a computer system using these half adder to solve the binary addition operation of two inputs. From the combination of half adder, we can find the full adder with a three input system. It can easily compute all type of data input as the using of addition system.